REMARKS

An unintentional mistake was made in the application as originally filed, wherein claims 21-30 were omitted. In the Second Preliminary Amendment filed March 22, 2001, the applicants attempted to address this matter by canceling claims 1-40 to avoid any confusion. The applicants thus believed that claims 41-60 were pending. However, the Examiner has renumbered the claims 41-60 to Claims 31-50 (apparently to fill in the missing claim numbers). The applicants are unfamiliar with the practice of renumbering claims prior to issuance, and, in fact, the same Examiner did not renumber claims in a related case Serial No. 09/368,710 wherein the same claims, including the gap of claims 21-30, was present.

However, to avoid further confusion and to make sure the proper dependence has been established for the claims presented in dependent form, the applicants have amended claims 41-60 to reflect the newly assigned claim numbers as identified in the Action. Accordingly, the amendments made to the claims herein are not made for the purposes of patentability, rather the amendments collectively, are made to clarify the numbering, broaden the claims, and to include yet otherwise unclaimed subject matter.

With respect to the restriction requirement, the applicants believe that the restriction as presented is improper. According to 35 U.S.C. §121, when a requirement for restriction is made, an Examiner must state the reasons why the inventions as claimed are independent and distinct. According to the MPEP §816, "[t]he particular reasons relied on by the examiner for holding that the inventions as claimed are either independent or distinct should be concisely stated. A mere statement of conclusion is inadequate. The reasons upon which the conclusion is based should be given."

The Examiner is apparently asserting that each independent claim presently pending in this application represents an independent and distinct invention. The only support given for this assertion is an indication of PTO classification. However, the applicants believe that, at least in this instance, a recitation of classification numbers is inadequate to support the reasons the Examiner restricted the claims. For example, the Examiner has identified both Species 'a' and Species 'f' as falling into class 438, subclass 238, without providing further reasons as why the

inventions warrant restriction. Likewise, Species 'g' and Species 'i' are classified in the same class and subclass.

Still further, subclass 238 (Species 'a' and 'f'), subclass 279 (Species 'c'), and subclass 241 (Species 'j') are all indented under subclass 197 (Species 'b'). Similarly, Species 'g', Species 'h', Species 'i', and Species 'k' are all indented under subclass 199. Subclasses 197 and 199 differ in that subclass 197 relates generally to MOSFET devices and subclass 199 relates to CMOS devices (which are merely complimentary MOSFETS). Accordingly, based upon the classification alone, the applicants cannot discern the reasons for the restriction. Further, it would appear to the applicants that Species 'b' is generic to Species 'a', 'c', 'f'', 'g', 'h', 'i', and 'j', and at a minimum, to Species 'a', 'c', 'f', and 'j' as the classifications identified by the Examiner for these Species are each indented under subclass 197 (the classification of Species 'b').

Still further, some of the classifications appear to applicants to be confusing. For example, Species 'j' is classified in subclass 241, which is indented under subclass 239. Subclass 239 is a process for making a FET transistor having combined therewith, a capacitor as a passive device. However, no capacitor structure is claimed in any of the claims identified by the Examiner as belonging to Species 'j'. In a similarly confusing manner, Species 'h' is classified in subclass 229. Subclass 229 is a process for making self aligned CMOS devices. While one could certainly use self aligning processing techniques to form the transistors in the claimed inventions, self-aligning processes are not being claimed per se in the claims identified by the Examiner as belonging to Species 'h'. Also, Species 'l' is classified in subclass 587, which is indented under subclass 584. Subclass 584 is directed to processes having a step of depositing electrically or thermally conductive material upon a semiconductive substrate. As above, while one may use electrically or thermally conductive materials in the fabrication of a device according to the claimed invention, the process of depositing conductive materials is not being claimed per se.

The applicant are not asserting that the claims are obvious variants of one another. Rather, the applicants are asserting that a proper response cannot be framed because the reasons

for the restriction are unclear. Accordingly, the applicants believe that the restriction is improper.

The applicants point out that, because of the amendments to the claims herein, Species 'a', 'd', 'e', and 'f' are moot because each claim in those Species has been cancelled.

Conclusion:

Applicants assert that the current restriction is improper because no reasoning meeting the requirements of MPEP §816 has been provided to support the Examiner's position for restricting the pending claims. Therefore, the applicants respectfully request that the election requirement be withdrawn.

The applicants respectfully submit that the pending claims represent allowable subject matter. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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Appendix A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

~~45~~35. (Amended) A method of fabricating a first inverter comprising:

providing a semiconductor of a first type conductivity;

~~doping the semiconductor to provide a first type conductivity;~~

forming a well of a second type conductivity in the semiconductor ~~having a second type conductivity;~~;

forming a first type transistor in the well, wherein the first type transistor has a first source, a first drain, and a first gate;

~~forming a second type transistor in the substrate outside of the well;~~

forming a first contact in the well in spaced relation to the first type transistor; ~~and~~

forming a second contact in the well in spaced relation to the first type transistor; ~~wherein the second contact is separated from the first contact by the first type transistor.~~;

coupling the first contact to a first voltage input; and

coupling the second contact to the first source.

~~46~~36. (Amended) The method of claim ~~45~~35, wherein forming a first contact comprises forming a first contact a first distance from the ~~second~~ first ~~type transistor~~ source, wherein the first distance ~~determines~~ defines a first component of a parasitic resistance of the well; and

wherein forming a second contact comprises forming a second contact a second distance from the ~~second~~ first ~~type transistor~~source, wherein the second distance ~~determines~~ defines a second component of the parasitic resistance of the well.

~~47~~37. (Amended) The method of claim ~~45~~35 wherein:

-forming a well comprises forming an n-type well in the semiconductor;~~wherein~~

forming a first type transistor comprises forming a first p-type region in the well ~~for~~ defining ~~a~~ the first source, forming a second p-type region in the well ~~for~~defining ~~a~~ the first drain and forming ~~a~~ the first gate over the well~~, and wherein~~

~~forming a second type transistor comprises forming a first n-type region in the substrate for a source, forming a second n-type region in the substrate for a drain and forming a gate over the substrate~~.

~~48~~38. (Amended) A method for fabricating a memory cell comprising:

providing a semiconductor;

doping the semiconductor to provide p-type conductivity;

forming a first inverter, wherein forming a first inverter comprises:

forming a well in the semiconductor having a n-type conductivity;

forming a p-type transistor in the well;

forming a n-type transistor in the substrate outside of the well;

forming a first contact in the well; and

forming a second contact in the well, wherein the second contact is separated from the first contact by the ~~second~~p-type transistor;

forming a second inverter, wherein forming a second inverter comprises:

forming a well in the semiconductor having a n-type conductivity;

forming a p-type transistor in the well;

forming a n-type transistor in the substrate outside of the well;

forming a first contact in the well; and

forming a second contact in the well, wherein the second contact is separated from the first contact by the ~~second~~ p-type transistor; and

cross coupling the second inverter to the first inverter.

~~52~~42. (Amended) A method of fabricating a memory cell comprising:

providing a substrate;

forming a first semiconductor structure within the substrate;

forming a first pull-up transistor ~~within the first semiconductor structure by forming~~ having a first source and a first drain in the ~~substrate~~ first semiconductor structure, and ~~forming~~ a first gate over the ~~substrate~~first semiconductor structure;

forming a first pull-down transistor ~~within the first semiconductor structure by forming~~ having a second source and a second drain in the substrate, and ~~forming~~ a second gate over the substrate;

forming a first contact and a second contact within the first semiconductor structure, each of the first and second contacts positioned in spaced relation to the first pull-up transistor;

coupling the first drain to the second drain;

coupling the first gate to the second gate; ~~and~~

coupling the first source to the second contact; and

coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through a parasitic resistance of the first semiconductor structure.

~~53~~43. (Amended) A method of fabricating a memory cell comprising:

providing a substrate;

forming a first semiconductor structure and a second semiconductor structure within the substrate;

forming a first pull-up transistor ~~within the first semiconductor structure by forming~~ having a first source and a first drain in the ~~substrate~~ first semiconductor structure and ~~forming~~ a first gate over the ~~substrate~~first semiconductor structure;

forming a first pull-down transistor ~~within the first semiconductor structure by forming~~ having a second source and a second drain in the substrate and ~~forming~~ a second gate over the substrate;

forming a first contact and a second contact within the first semiconductor structure;

forming a second pull-up transistor ~~within the second semiconductor structure by forming~~having a third source and a third drain in the ~~substrate~~ second semiconductor structure and ~~forming~~ a third gate over the ~~substrate~~second semiconductor structure;

forming a second pull-down transistor ~~within the first semiconductor structure by forming~~ having a fourth source and a fourth drain in the substrate, and ~~forming~~ a fourth gate over the substrate;

forming a third contact and a fourth contact within the second semiconductor structure;

coupling the first drain to the second drain and the third drain to the fourth drain;

coupling the first gate to the second gate and the third gate to the fourth gate;

coupling the first source to the second contact; ~~and~~

coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure; ~~and~~

coupling the third source to the fourth contact; and

coupling the third contact to the first voltage input such that the ~~first~~ third source is coupled to the first voltage input through parasitic resistance of the second semiconductor structure.

~~54~~44.(Amended) The method of claim ~~53~~43, further comprising:

doping the substrate to form a p-type conductivity; and

forming a n-type well within the first semiconductor structure.

~~55~~45. (Amended) The method of claim ~~54~~44, further comprising forming a n-type well within the second semiconductor structure.

~~56~~46. (Amended) A method of fabricating an SRAM memory array comprising:

providing a substrate;

forming a plurality of memory cells arranged in rows and columns, each of the plurality of memory cells fabricated by:

forming a first semiconductor structure within the substrate;

forming a second semiconductor structure within the substrate;

forming a first pull-up transistor ~~within the first semiconductor structure by forming a~~having first source and a first drain in the ~~substrate~~ first semiconductor structure and ~~forming~~ a first gate over the ~~substrate~~first semiconductor structure;

forming a first pull-down transistor ~~within the first semiconductor structure by forming~~having a second source and a second drain in the substrate and ~~forming~~ a second gate over the substrate;

forming a first contact and a second contact within the first semiconductor structure;

forming a second pull-up transistor ~~within the second semiconductor structure by forming~~having a third source and a third drain in the ~~substrate~~ second semiconductor structure and ~~forming~~ a third gate over the ~~substrate~~second semiconductor structure;

forming a second pull-down transistor ~~within the first semiconductor structure by forming~~having a fourth source and a fourth drain in the substrate and ~~forming~~ a fourth gate over the substrate;

forming a third contact and a fourth contact within the second semiconductor structure;

forming a first terminal and a second terminal of a first access transistor in the substrate;

forming a third terminal and a fourth terminal of a second access transistor in the substrate

coupling the first drain to the second drain and the third drain to the fourth drain;

coupling the first gate to the second gate and the third gate to the fourth gate;

coupling the first terminal to the first and second drains;

coupling the third terminal to the third and fourth drains;

coupling the first source to the second contact; ~~and~~

coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure; ~~and~~

coupling the third source to the fourth contact; and

coupling the third contact to the first voltage input such that the ~~first~~ third source is coupled to the first voltage input through parasitic resistance of the second semiconductor structure;

coupling the first and second access gates of each of the plurality of memory cells to respective row lines;

coupling the second terminals of each of the plurality of memory cells to respective first column lines; and

coupling the fourth terminals of each of the plurality of memory cells to respective second column lines.

~~57~~47. (Amended) A method of fabricating a memory device comprising:

forming a first semiconductor structure having a first type region and second type region;

forming a first pull-up transistor ~~within the first semiconductor structure by forming~~having a first source~~,~~ and a first drain in the first type region and a first gate over the first type region;

forming a first pull-down transistor ~~within the first semiconductor structure by forming~~having a second source and a second drain in the second type region~~,~~ and a second gate over the second type region;

forming a first contact and a second contact within the first semiconductor structure;

coupling the first drain to the second drain;

coupling the first gate to the second gate; and

coupling the first source to the second contact; and

coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure.

~~58~~48. (Amended) A method of fabricating a memory device:

forming a first semiconductor structure having a first type region and a second type region and a second semiconductor structure having a first type region and a second type region;

forming a first pull-up transistor within the first semiconductor structure by forming a first source~~,~~ and a first drain in the first type region~~,~~ and a first gate over the first type region;

forming a first pull-down transistor within the first semiconductor structure by forming a second source~~,~~ and a second drain in the second type region~~,~~ and a second gate over the second type region;

forming a first contact and a second contact within the first semiconductor structure;

forming a second pull-up transistor within the second semiconductor structure by forming a third source~~,~~ and a third drain in the first type region~~,~~ and a third gate over the first type region;

forming a second pull-down transistor within the ~~first~~ second semiconductor structure by forming a fourth source~~,~~ and a fourth drain in the second type region , and a fourth gate over the second type region;

forming a third contact and a fourth contact within the second semiconductor structure;

coupling the first drain to the second drain and the third drain to the fourth drain;

coupling the first gate to the second gate and the third gate to the fourth gate;

coupling the first source to the second contact; ~~and~~

coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure; ~~and~~

coupling the third source to the fourth contact; and

coupling the third contact to the first voltage input such that the ~~first~~ third source is coupled to the first voltage input through parasitic resistance of the second semiconductor structure.

~~59~~49. (Amended) The method of claim ~~58~~48, further comprising: ~~—~~

~~doping the substrate to form a p-type conductivity; and~~

~~—~~forming a n-type well within the first semiconductor structure.

~~60~~50. (Amended) A method of fabricating a memory device comprising:

forming a plurality of memory cells arranged in rows and columns, each of the plurality of memory cells fabricated by:

forming a first semiconductor structure having a first type region and a second type region;

forming a second semiconductor structure having a first type region and a second type region;

forming a first pull-up transistor within the first semiconductor structure by forming a first source~~,~~ and a first drain in the first type region~~,~~ and a first gate over the first type region ;

forming a first pull-down transistor within the first semiconductor structure by forming a second source~~,~~ and a second drain in the second type region and a second gate over the second type region ;

forming a first contact and a second contact within the first semiconductor structure;

forming a second pull-up transistor within the second semiconductor structure by forming a third source and ~~,~~a third drain in the first type region~~,~~ and a third gate in the second type region;

forming a second pull-down transistor within the ~~first~~ second semiconductor structure by forming a fourth source~~,~~ and a fourth drain in the second type region~~,~~ and a fourth gate over the second type region;

forming a third contact and a fourth contact within the second semiconductor structure;

forming a first terminal and a second terminal of a first access transistor in the substrate;

forming a third terminal and a fourth terminal of a second access transistor in the substrate

coupling the first drain to the second drain and the third drain to the fourth drain;

coupling the first gate to the second gate and the third gate to the fourth gate;

coupling the first terminal to the first and second drains;

coupling the third terminal to the third and fourth drains;

coupling the first source to the second contact; ~~and~~

coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure; ~~and~~

coupling the third source to the fourth contact; ~~and~~

coupling the third contact to the first voltage input such that the ~~first~~ third source ~~is~~ coupled to the first voltage input through parasitic resistance of the second semiconductor structure;

coupling the first and second access gates of each of the plurality of memory cells to respective row lines;

coupling the second terminals of each of the plurality of memory cells to respective first column lines; and

coupling the fourth terminals of each of the plurality of memory cells to respective second column lines.